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United States Patent [19]

Khan et al.

[11] **Patent Number: 5,598,052**

[45] **Date of Patent: Jan. 28, 1997**

[54] **VACUUM MICROELECTRONIC DEVICE AND METHODOLOGY FOR FABRICATING SAME**

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[73] Assignee: **Philips Electronics North America**, New York, N.Y.

[21] Appl. No.: **359,249**

[22] Filed: **Dec. 16, 1994**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 177,089, Dec. 30, 1993, Pat. No. 5,438,343, which is a continuation-in-part of Ser. No. 922,707, Jul. 28, 1992, abandoned.

[51] **Int. Cl.**^{6} **H01J 21/10**

[52] **U.S. Cl.** **313/310**; 313/495; 313/309; 313/336

[58] **Field of Search** .... 313/309, 310, 313/336, 351, 495, 496, 493, 477 R, 582, 610, 616

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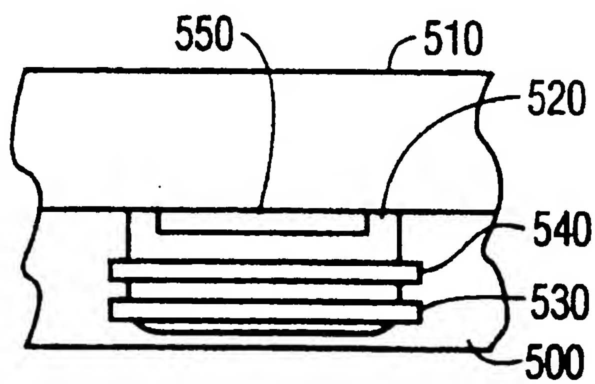
Primary Examiner—Nimeshkumar Patel
Attorney, Agent, or Firm—John C. Fox

[57] **ABSTRACT**

A vacuum state microelectronic device comprising at least a cathode, an anode, and a grid, disposed in a cavity, and formed by the wafer bonding of two planar substrates. The technology permits multiple vacuum state microelectronic devices (vacuum tubes) to be arrayed on a single substrate in an integrated manner. So as to form a bond as strong as the substrate itself.

11 Claims, 12 Drawing Sheets



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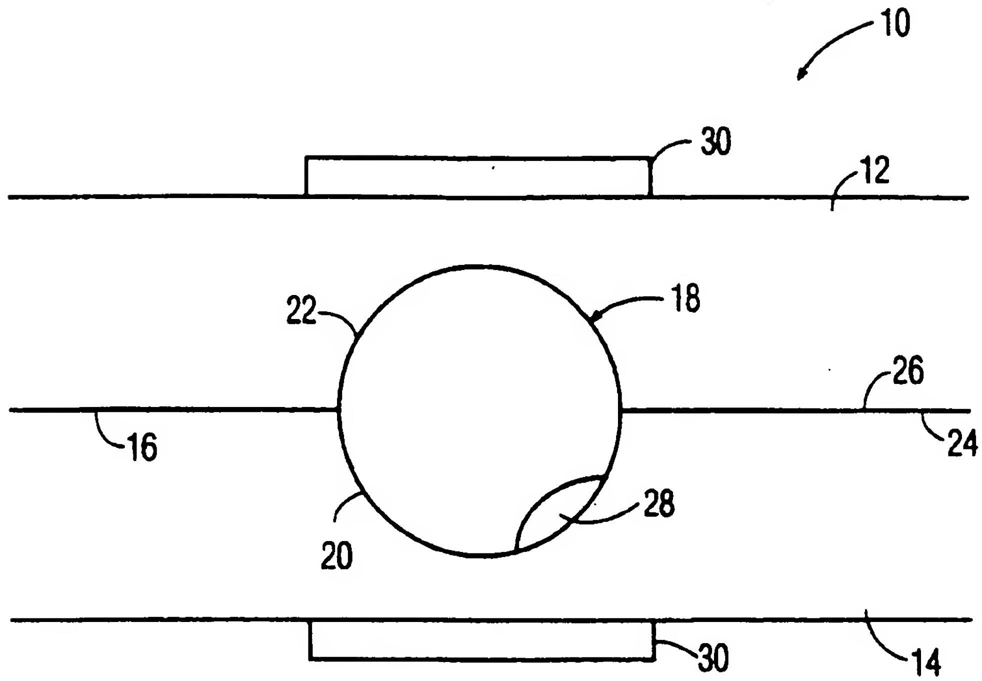

FIG. 1

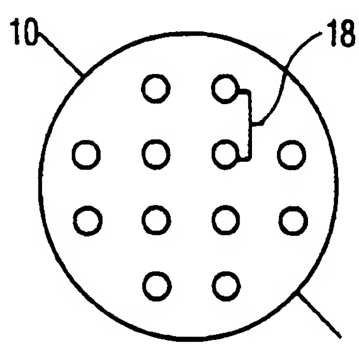

FIG. 2

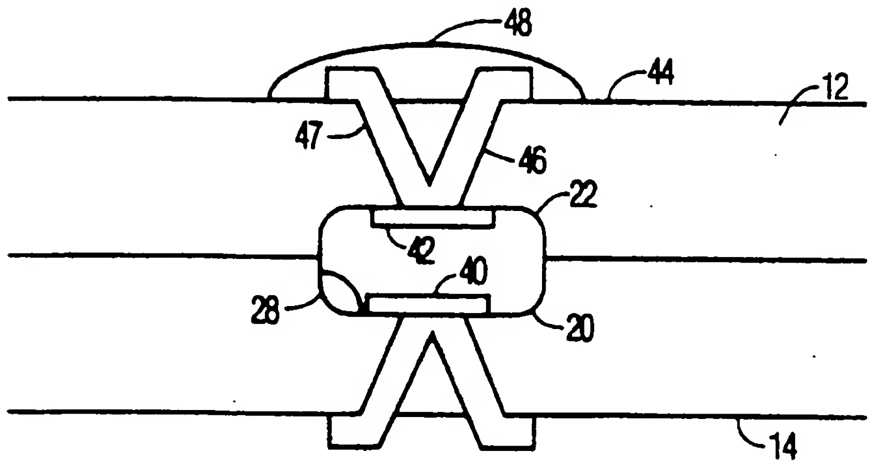

FIG. 3

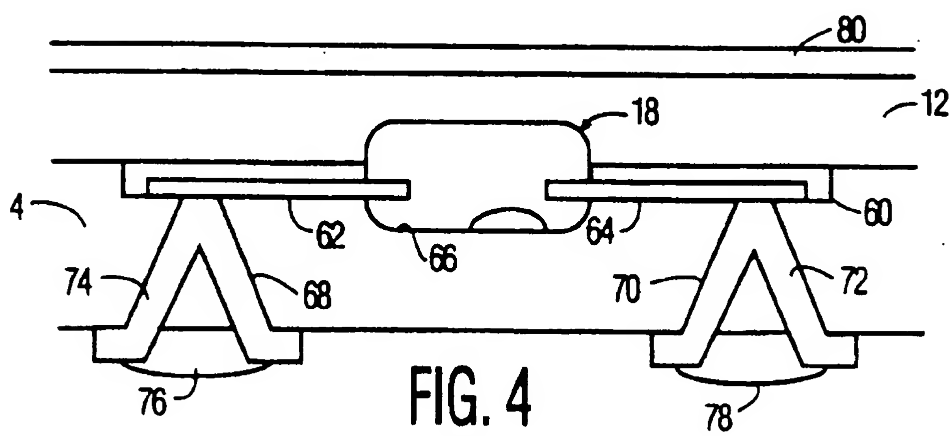

FIG. 4

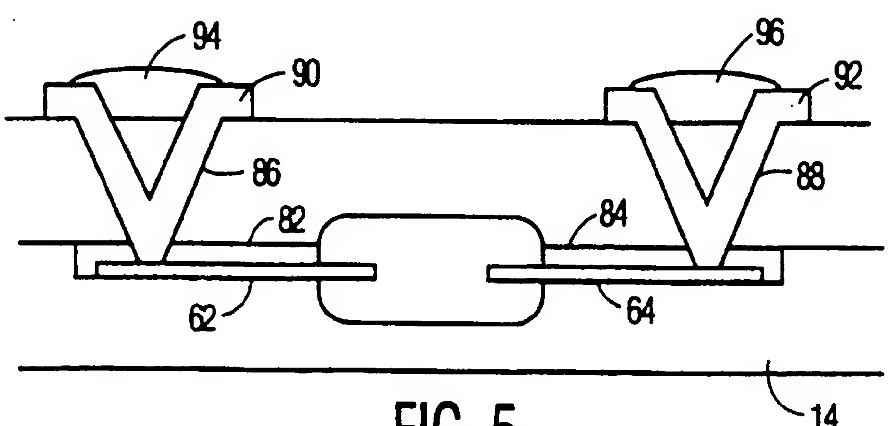

FIG. 5

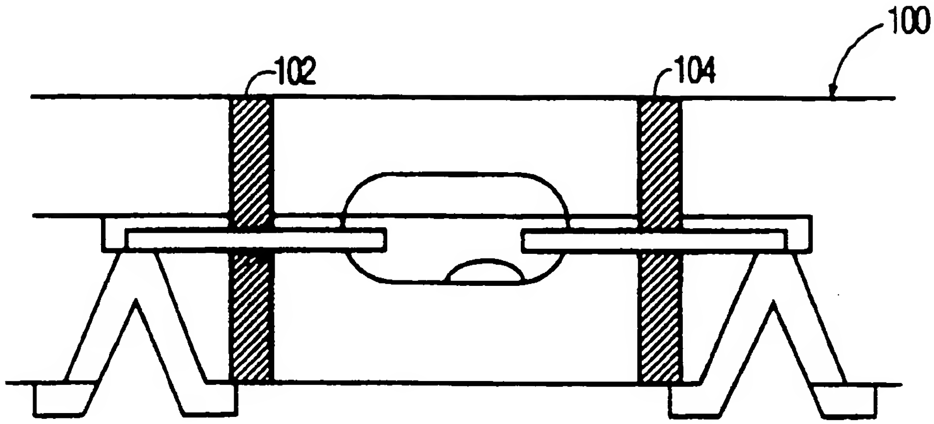

FIG. 6

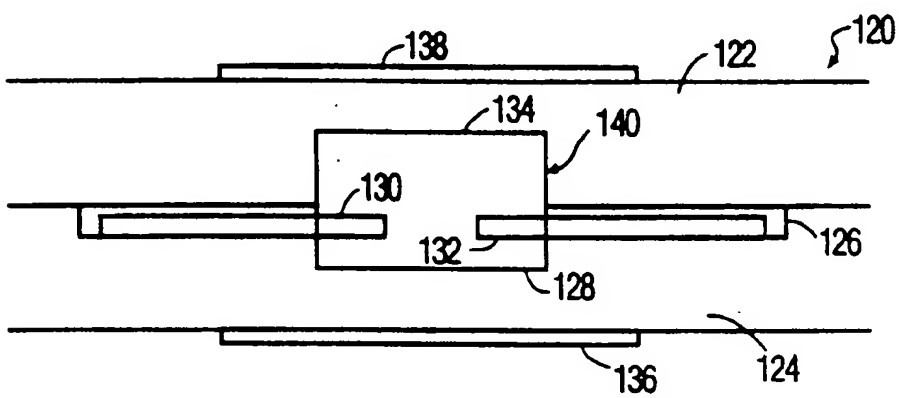

FIG. 7

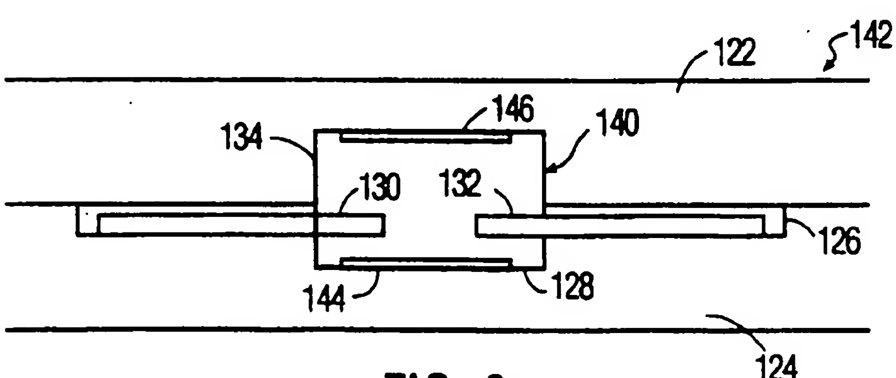

FIG. 8

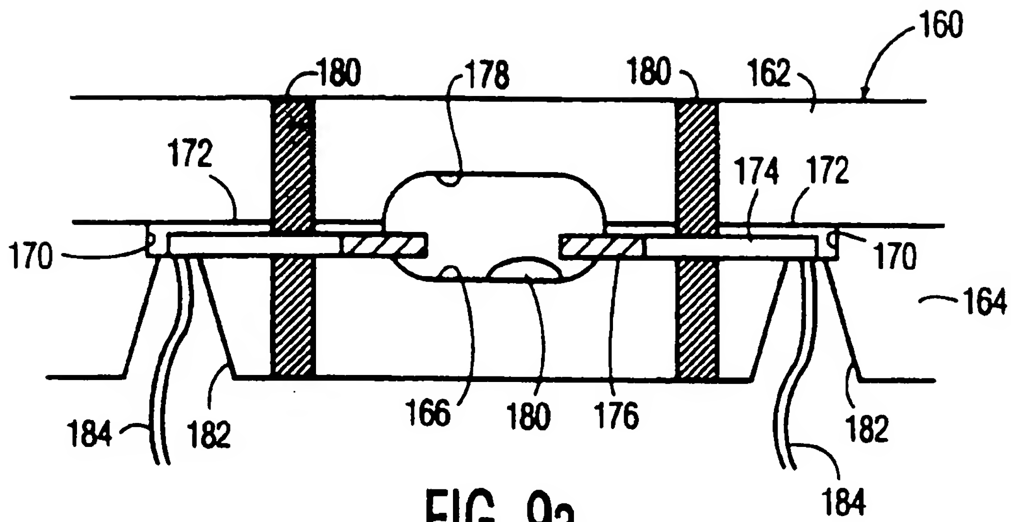
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FIG. 9a

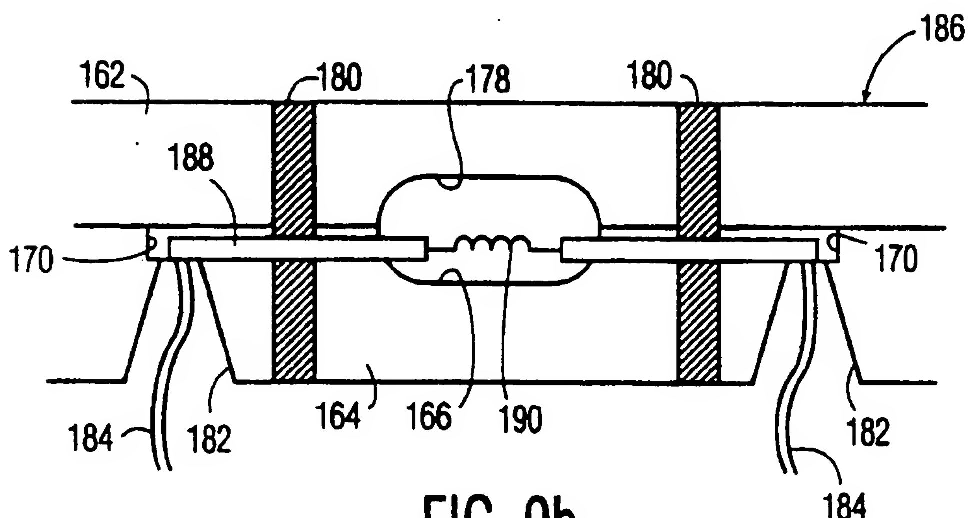
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FIG. 9b

FIG. 10a

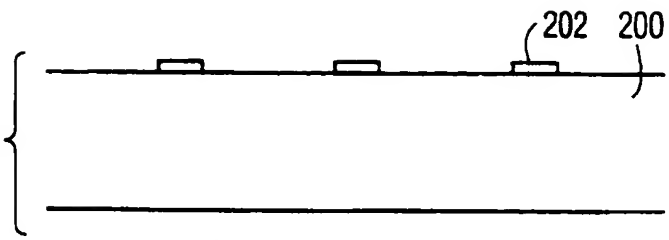

FIG. 10b

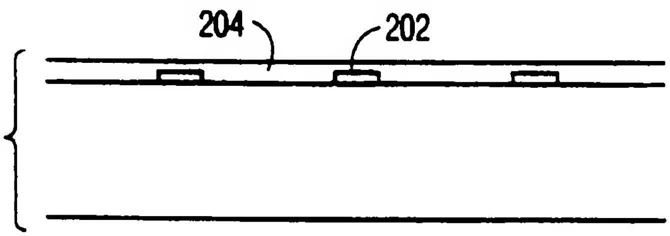

FIG. 10c

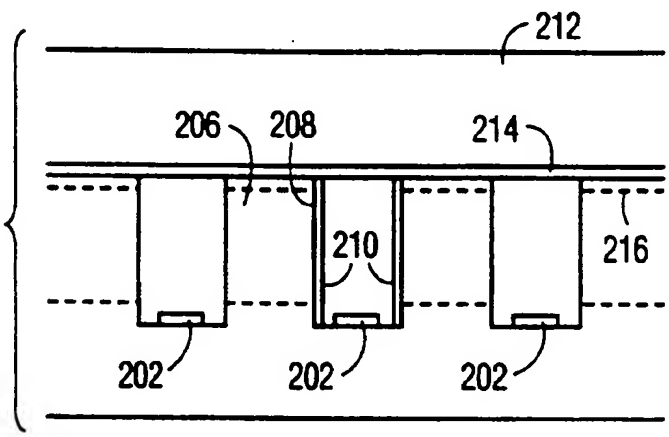

FIG. 10d

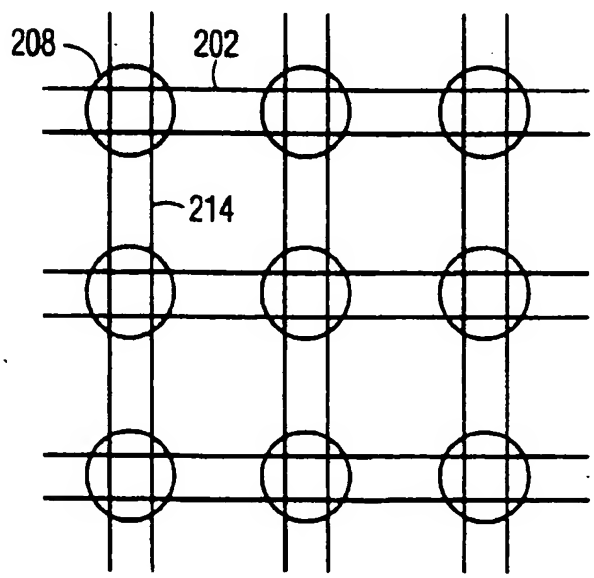

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FIG. 11a

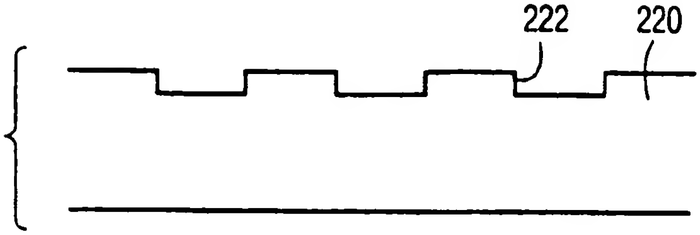


FIG. 11b

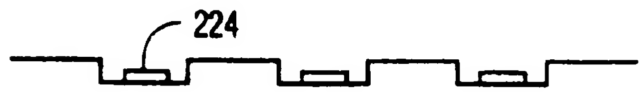


FIG. 11c

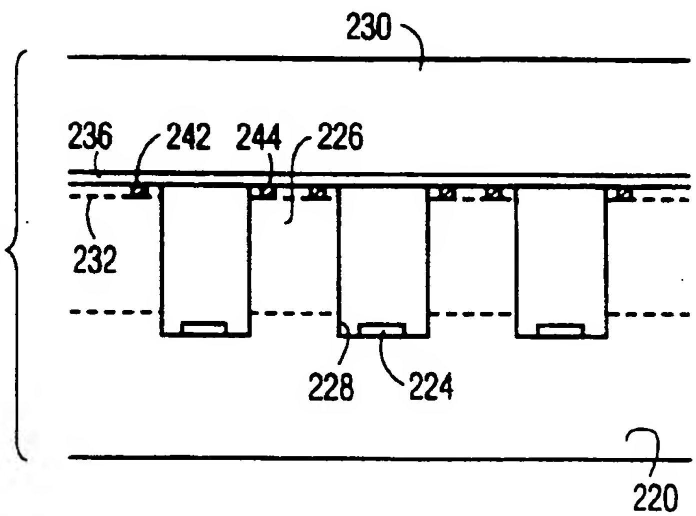


FIG. 11d

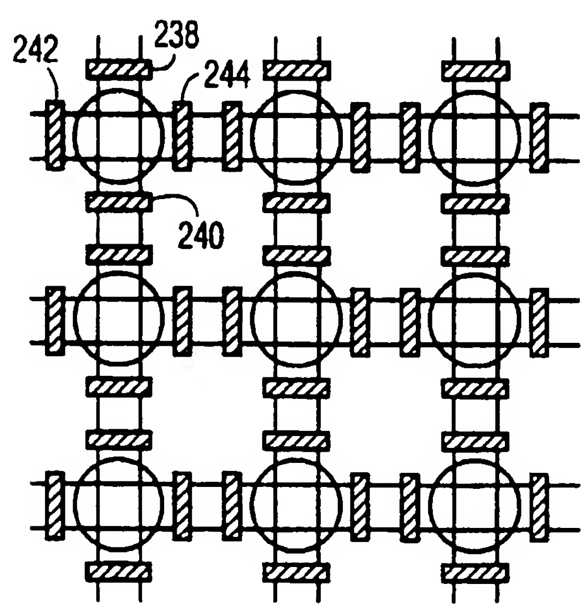


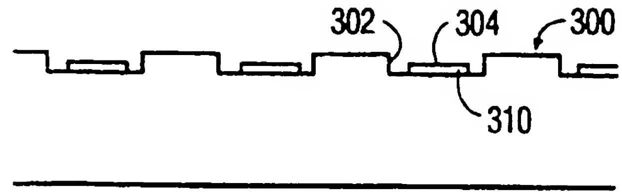
FIG. 12a


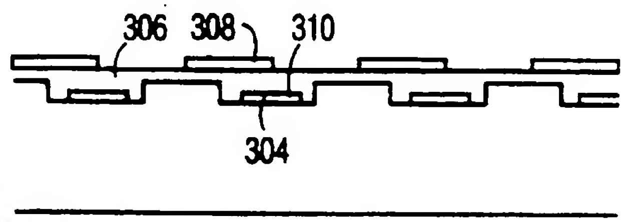
FIG. 12b


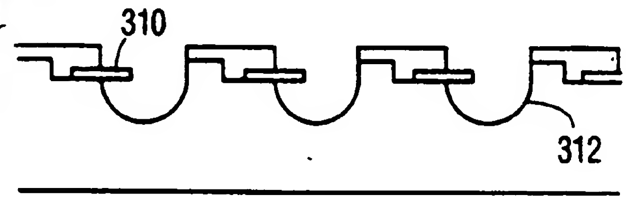
FIG. 12c


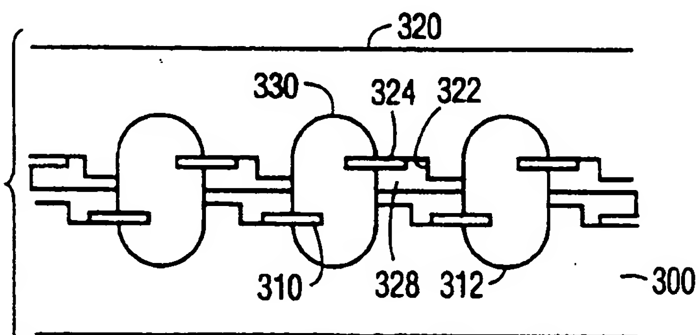
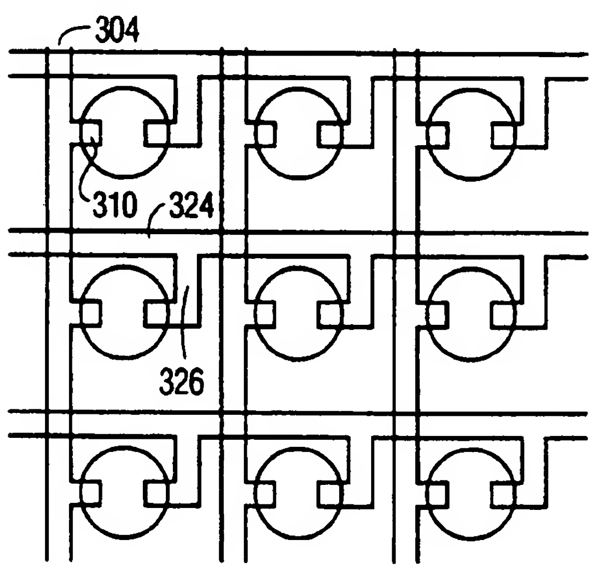
FIG. 12d


FIG. 12e


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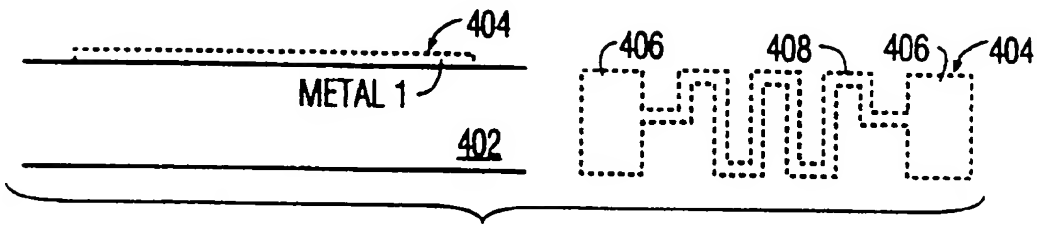

FIG. 13a

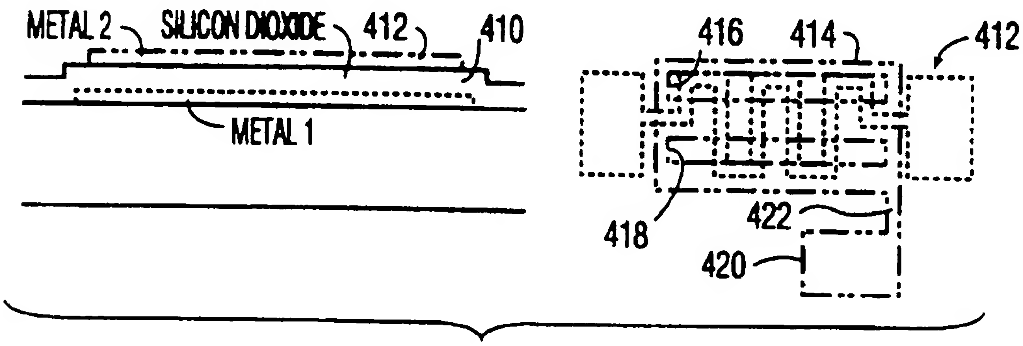

FIG. 13b

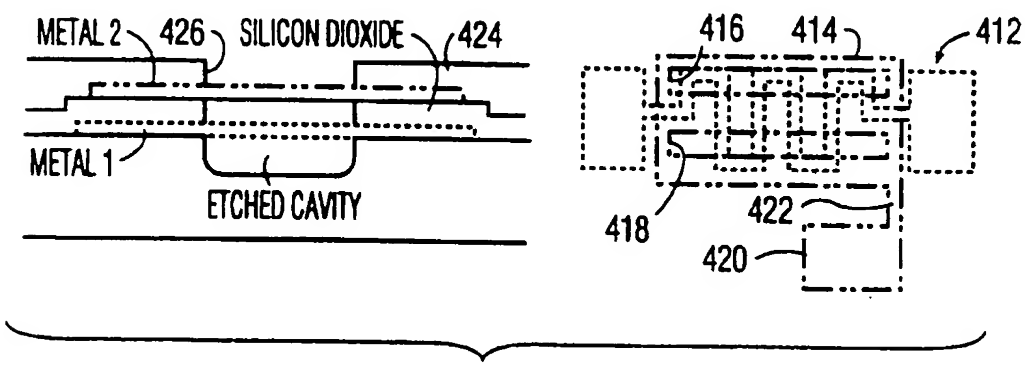

FIG. 13c

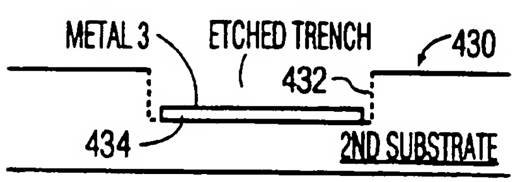

FIG. 13d

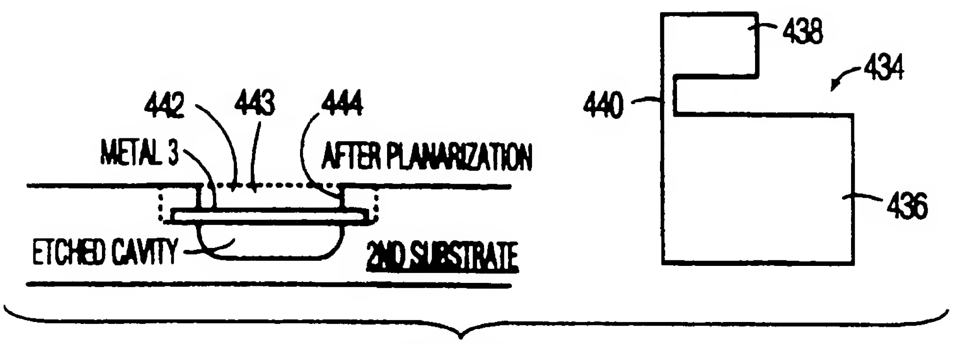

FIG. 13e

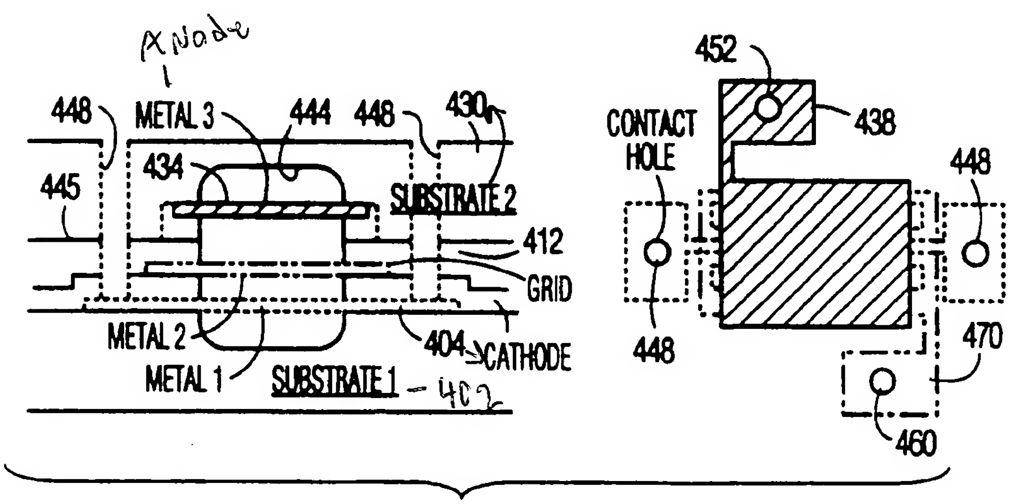

FIG. 13f

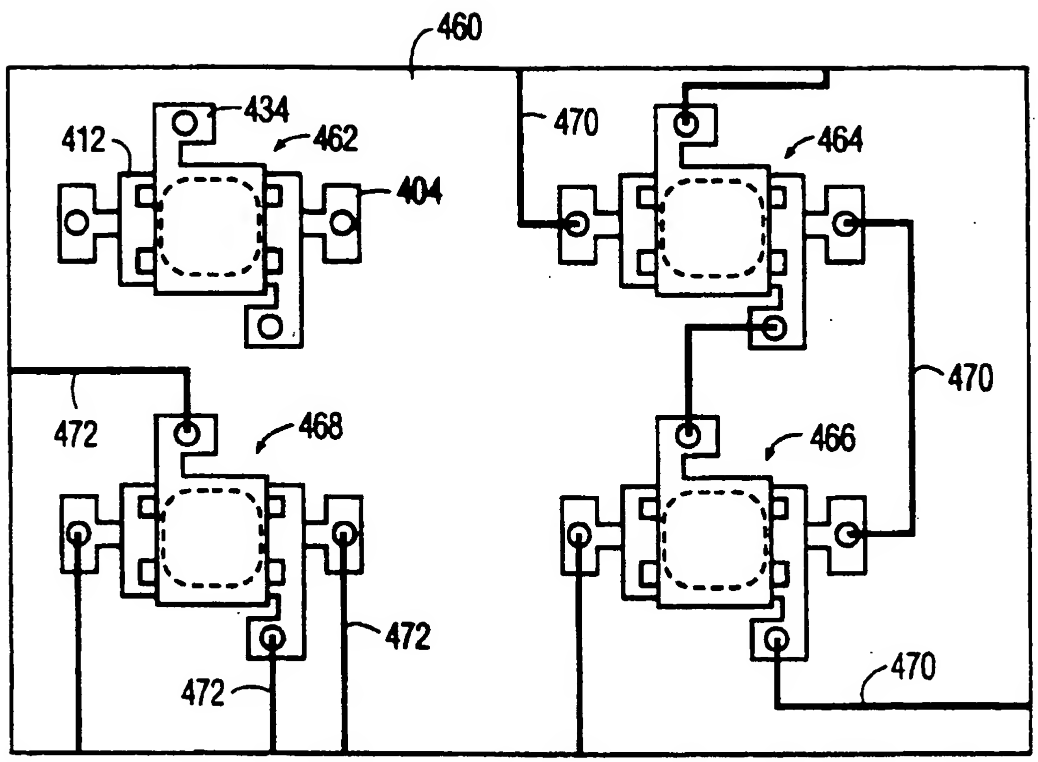

FIG. 14

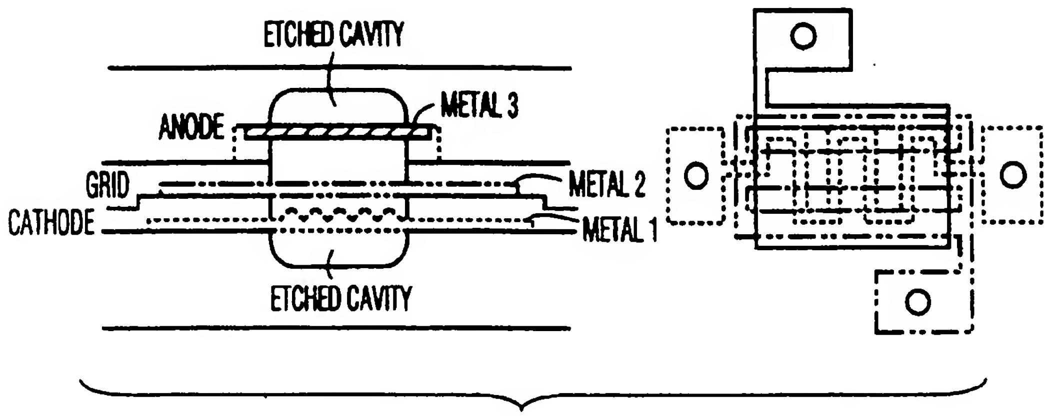
ETCHED CAVITY
METAL 3
ANODE
GRID
METAL 2
CATHODE
METAL 1
ETCHED CAVITY

FIG. 15

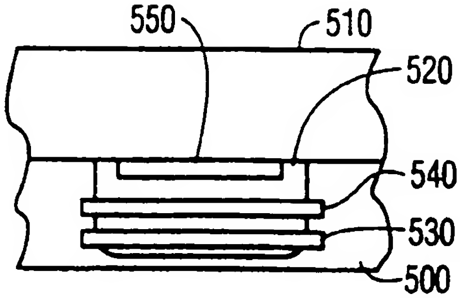

FIG. 16a

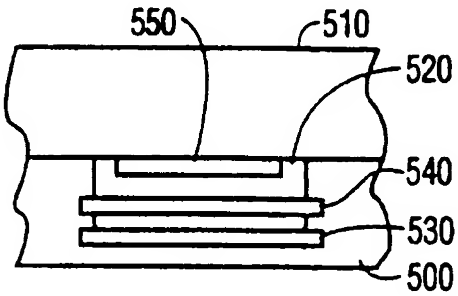

FIG. 16b

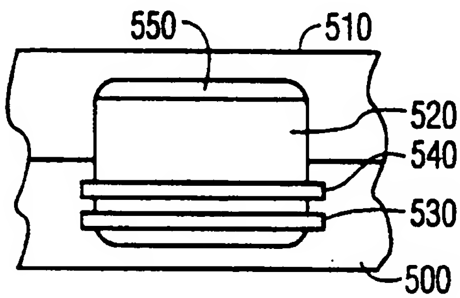

FIG. 16c

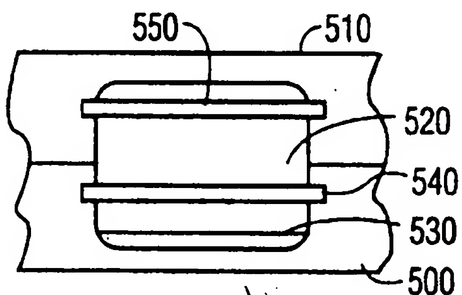

FIG. 16d

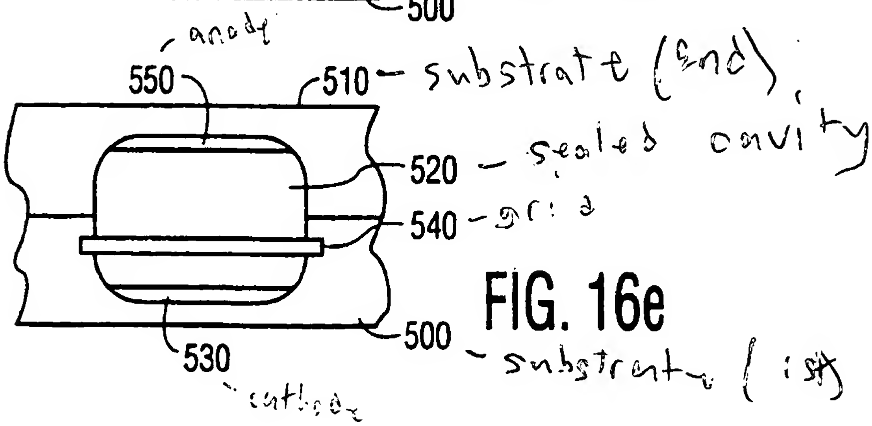

FIG. 16e

VACUUM MICROELECTRONIC DEVICE AND METHODOLOGY FOR FABRICATING SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of application Ser. No. 177,089 filed Dec. 30, 1993 now U.S. Pat. No. 5,438,343 which in turn is a continuation-in-part of application Ser. No. 922,707 filed Jul. 28, 1992 now abandoned.

BACKGROUND AND SUMMARY OF THE INVENTION

This application is directed to vacuum microelectronic devices and methodology for producing such devices, having first and second substrates capable of withstanding heat and pressure; at least one of the substrates having at least one cavity with electrodes deposited in the cavity; the first and second substrates wafer bonded together such that the substrates are joined together at all points of contact.

Lamps

Gas discharge lamps (mercury vapor, sodium vapor, metal halide) are an important segment of the lighting industry. It is well known that the luminous efficacy of gas discharge lamps increases substantially at high pressures (1–200 atmospheres). However, the containment of such high pressures in a transparent vessel has presented significant problems. Gas pressure is restricted in many instances because of the difficulty of finding materials that are sufficiently lightweight, while at the same time capable of withstanding high heat and pressures. Furthermore, such materials, to be practicable, must be capable of relatively inexpensive mass production. The usual construction of gas discharge lamps is to suspend a translucent pressure and heat resistant discharge vessel by means of a metal framework within an outer glass bulb.

The present invention provides an entirely new paradigm for the construction of high pressure gas discharge lamps and displays. Rather than a discharge vessel mechanically suspended within an outer bulb, the present invention is directed towards methods of fabricating high pressure "microlamps" utilizing micromachining techniques which are similar to integrated circuit fabrication techniques such as the etching of and bonding of planar substrates. The present invention is directed to an improved gas discharge lamp that can withstand very high pressures and the method of making such a lamp by means of integrated circuit manufacturing techniques. The lamp is manufactured from two planar sheets of temperature and pressure resistant transparent material. A cavity is etched in one or both of the sheets and electrodes are therefore deposited or placed in the cavity. The cavity is charged with a filler appropriate to the type of lamp being manufactured such as mercury, sodium or metal halides. The two sheets are then bonded together so as to seal the cavity within the sheets. Contact may then be made with the electrodes to activate the lamp. Electrodeless lamps activated by microwave energy may also be manufactured by this technique. Miniature gas discharge lasers may also be produced by this technique.

The term "bonding" as used throughout this application refers to "wafer bonding" techniques used in the manufacture of integrated circuits and sensors. Such techniques generally comprise anodic or fusion bonding which results in a chemical bond at the interface which is as strong as the bulk material. This bond permits the fabrication of cavities

which can withstand extremely high pressures (greater than 200 atmospheres). In this technique, a bond is present at all points of contact between the substrate surfaces, so that each cavity is individually sealed.

There are two types of wafer bonding processes. Anodic wafer bonding or fusion wafer bonding. Fusion wafer bonding: In this process two flat wafers (e.g. quartz) are prepared with hydrophilic surfaces and brought into contact. The Van de Waal's forces pull the two wafers together and result in a bond at the interface. The two wafers are then annealed at high temperature (e.g. 1000 C.), resulting in a chemical bond at the interface, which has the strength of the bulk material. Even though the temperature is elevated, bonding takes place at a temperature below the melting point of the material (quartz: approximately 1400° C.). This means that the substrate will not deform during the bonding process. Anodic wafer bonding: In this process, two flat wafers are brought into contact as in the fusion wafer bonding process. However, the annealing is carried out at lower temperatures and with an electric field applied across the wafers. This process is useful for materials that have mobile ions and cannot be annealed at high temperatures (such as glass). The electric field results in the collection of positive and negative charges at the interface, which lead to high electric fields, which pull the wafers together. This process is more forgiving of the degree of wafer flatness, but is more difficult to implement and does not work with materials that are free of mobile ions.

The present development has implications for fluorescent lamps as well. Fluorescent lamps fabricated by using wafer bonding will not only be much sturdier, but the internal pressures can exceed 1 atmosphere. This is because flat fluorescent lamps made by the present technology will be bonded everywhere, except where the discharge space is located. As noted above, this bond will have the strength of the bulk material. This allows the lamp to be optimized in a sub-normal "glow" discharge mode, where the optimum pressure for the discharge can exceed 1 atmosphere for short electrode spacing or narrow walls. Glass frit sealing (at the edges) in the prior art is a mechanical process, which cannot easily be used to make small individually sealed cavities (e.g. 100 micron diameter) and which is not a batch production process. On the other hand, the wafer bonding process can be used with IC techniques to make extremely small individually sealed cavities (<100 micron diameter) and is a batch process which is fully compatible with IC techniques. The present development also permits the phosphors that fluoresce to be located either inside the discharge cavity (as in current fluorescent tubes) or outside of the cavity.

Displays

Emissive, large area displays are expected to have applications in the large flat panel television market, particularly for high definition television. Plasma displays are promising candidates for this application. Plasma displays are constructed by patterning orthogonal electrodes on glass substrates, placing spacers between the glass substrates, sealing the substrates at the periphery and filling the space in between the substrates with the working gas. In another version of a plasma panel, a glass sheet with holes cut through it is placed between electrode substrates. As a result, individual discharges are confined to the holes in the middle sheet. However, the seal is still made at the periphery and the gas is filled from a small opening at the periphery, which is thereafter sealed. In both types of structures, however, the individual pixels are not sealed from each other. Such conventional plasma displays or back-lights are shown in

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Patent Publications WO 90/09676, WO 87/04562, EP 0,302,748 and EP 0,467,542 A2.

Since the conventional displays are large, the gas fill pressure cannot be much more than one atmosphere, as the forces on the glass substrate are too great and will either force the substrates apart, or shatter them. For example, in a panel measuring 1200 sq in (30×40 in), only 0.1 psi of pressure over 1 atmosphere will result in an outward force of 120 lbs on each substrate. Therefore, the gas fill in these substrates must be restricted to a maximum pressure of 1 atm. At the same time, one of the key problems plaguing the plasma panels is low brightness for TV applications because of the lower pressure at which they must be operated.

This application is directed to a display technology based on micromachining, that will yield bright, efficient and rugged displays for TV applications. In this construction, the individual pixels are completely isolated from each other. The individual pixels are formed by etching and bonding of the transparent substrates (glass, fused quartz, sapphire, PCA or others), so that the pixels are comprised of sealed cavities containing electrodes and the ambient gas or dosing material. Since each pixel is a sealed cavity, which is formed by bonding the etched substrates, the bonded interface is as strong as the bulk of the substrate and the pressure within such a pixel can be substantially more than one atmosphere.

The improved construction can readily provide higher pressure discharges, which can emit substantially more light. This is particularly advantageous for HDTV applications, where pixel sizes need to be small (<300 μm), even for large area displays. However, it is difficult to use mechanical processes economically to make small but deep apertures. Furthermore dry chemical etching processes are too slow and also too expensive. Therefore, the pixel cavities must be made by wet chemical etching, which is isotropic and results in etched cavities whose lateral dimensions are roughly twice the depth. Therefore, the spacing between electrodes must be kept small. However, in order to optimize the UV radiation from xenon, it has been demonstrated that the ratio of electric field to pressure (E/p) is 7–8 V/cm.torr. Therefore, for driving voltages of 60 V and electrode spacings less than 100 μm, the optimum pressure is more than one atmosphere which is not obtainable with prior manufacturing processes.

Although, the discussion so far has assumed that the discharges are in the "glow" phase, another advantage of this technology is that the pixels can be operated as high pressure arc lamps. It is well known that these high pressure arc lamps have significant output in the visible wavelength range of the electromagnetic spectrum. Therefore, the pixels can be used with color filters to form a display, thus avoiding the use of phosphors. When the discharge is operated in the "glow" phase, the electrodes do not get very hot, however, when the discharge is operated in the "arc" phase, the electrodes get hot, thus the choice of the metal for the electrodes is a function of the desired operating range. Additionally, in the arc phase, reignition is a problem, but it can be avoided by use of an auxiliary discharge, which is hidden from view, but connected to the display discharge space as was done in prior panels.

U.S. Pat. No. 4,990,826 is directed to a display device. In this patent, channels are formed by etching through one plate and placing it in contact with two plates on which electrodes have been formed. The three plates are then sealed together by heating. Because of the electrodes, the seal can only be formed by softening the glass so it can flow around the metal electrode and form a seal. Such heating may unacceptably deform the entire structure. This patent, a vacuum port is also sealed into the device with glass frit. The discharge

space is evacuated and filled through this port and then sealed by melting the pumping port tube.

The discharge space in the present invention is formed by wafer bonding two or more plates together. In the present electroded lamps, the electrodes are sealed and the surface of the wafer is planarized by using wafer planarizing methods to deposit glass or SiO_2 films. The planarized wafers are then bonded together to seal the discharge space. Since the wafer bonding is carried out in the atmosphere required in the discharge space (e.g. Ar, Ne, Xe, etc.), the atmosphere is sealed into the cavity and a port is not required. Therefore, the present process allows the formation of many individually sealed cavities on one substrate, whereas the process described in U.S. Pat. No. 4,990,826 does not. The present process has the advantages of batch processing whereas the prior art does not. The formation of a seal by wafer bonding also has practical advantages over glass softening, in that the structure will not deform during wafer bonding but will during softening of the glass as in U.S. Pat. No. 4,990,826.

Vacuum Microelectronic Devices

Vacuum Microelectronics is the name given to the emerging technology of microelectronic "vacuum state" devices. Since these devices are based on the motion of electrons in vacuum, they are expected to be much faster than solid state devices in which the electron drift velocity is slower. In addition to higher speed, vacuum microelectronic devices are expected to be significantly more radiation hard. In the old vacuum "tube" technology, the electrons moved in a vacuum, but the devices were much larger and transmit distances much greater, so that technology was quickly replaced by solid state technology, where solid state devices could meet the performance requirements. Therefore, if "vacuum state" devices could be downsized to the small-size of solid state devices, it would be a significant advantage.

The basic vacuum tube device, the classic triode, however, is based on thermionic emission and it is generally believed that the high temperatures and high power dissipation required for satisfactory operation are not acceptable in any microelectronic structure. Therefore, the vacuum microelectronic devices developed to date are based on a "cold" emission process: field assisted emission. These devices are based on emission from sharp points of suitable materials or from reverse biased shallow junction diodes. The equivalent of the cathode is the pointed emitter (cold cathode), which emits electrons, which are collected by an anode and modulated by a grid. These devices are in the early stages of research and have yet to demonstrate significant results. The structures that have been fabricated have to be placed in a vacuum chamber to be tested.

This application is directed to a new technology for vacuum state devices, which not only allows the fabrication of individually sealed vacuum microdevices, in which the vacuum space is closed and sealed so that a vacuum chamber is not required for their operation, but also allows the fabrication of vacuum microdevices based on thermionic emission (hot cathodes), which operate at high temperatures, which is not the case with existing approaches to vacuum microelectronics.

This technology is based on the formation of cavities in one or both of a pair of substrates, followed by alignment and wafer bonding of the substrates to seal the cavities. The basic structure, which is the equivalent of the traditional triode, is fabricated by using a process sequence similar to those used in our previous applications to form light emitting devices. The substrate may be of any material suitable for wafer bonding, such as quartz, sapphire, silicon or glass, depending on the anticipated operating conditions of the

device. The wafer bonding process used can either be fusion bonding or anodic bonding, also depending on the substrate. Similar bonding processes are widely used in sensor applications.

In the first step, a first electrode of an electron emissive material, such as W, Mo, other refractory metal or a silicide, is deposited on a first substrate and patterned. An intermediate layer of silicon dioxide is then deposited (by CVD, PECVD, SILOX or other methods) followed by another electrode which is deposited and patterned. The distance between the first and second electrodes can be adjusted simply by varying the thickness of the silicon dioxide. This distance will be, for example, the distance between the cathode and the grid. A second intermediate layer is then deposited, and the wafer is then planarized by reflowing of the layer or by any other planarizing method. A cavity is then etched around the electrodes, by using photolithography and selective etching.

A third electrode, for example, the anode, is deposited on a second substrate. The second substrate is then planarized, aligned and bonded to the first, in a vacuum environment, resulting in a sealed cavity containing a vacuum environment. The fusion or anodic bonding results in a chemical bond at the interface, which has the strength of the bulk material. Contact holes to the electrodes are then opened up by either etching or "drilling" with a laser.

Preferably, the third electrode is deposited and patterned inside a trench, which is etched on the second substrate. The trench is then filled, and planarized, after which a cavity surrounding the electrode is formed by photolithography and etching, prior to bonding.

BRIEF DESCRIPTION OF THE DRAWINGS

For better understanding of the invention, reference is made to the following drawings which are to be taken in conjunction with the detailed description to follow:

FIG. **1** is a sectional diagram of an electrodeless, radio frequency activated lamp constructed in accordance with the present invention;

FIG. **2** is a plan view of the translucent substrates having a plurality of lamp cavities disposed therein;

FIG. **3** is a sectional view of a lamp having opposed electrodes manufactured in accordance with the present invention;

FIG. **4** is a sectional view of a side electrode lamp manufactured in accordance with the present invention; and

FIG. **5** is a sectional view of a further embodiment of a side electrode lamp constructed in accordance with the present invention.

FIG. **6** is a sectional view of a side electrode lamp including melt zones to further seal the electrodes;

FIGS. **7** and **8** are sectional views of micro-lasers constructed in accordance with the invention;

FIGS. **9***a* and **9***b* are sectional views of lamps constructed in accordance with the present invention using conventional electrodes;

FIGS. **10***a*–**10***d* illustrate a first construction for a gas discharge display panel in accordance with the present invention;

FIGS. **11***a*–**11***d* illustrate a second construction of a gas discharge display panel;

FIGS. **12***a*–**12***e* illustrate a third type of gas discharge display panel in accordance with the invention; and

FIGS. **13***a*–**13***f* illustrate a vacuum microelectronic device constructed in accordance with the invention with sectional views on the left and plan views on the right;

FIG. **14** is a plan view of a substrate containing multiple microelectronic vacuum devices and the interconnections therebetween;

FIG. **15** is an illustration of a point type microelectronic device constructed in accordance with the present invention; and

FIGS. **16***a*–*e* illustrate variations of the device configuration shown in FIGS. **13***a*–*f*.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Light Emitting Devices

FIGS. **1** and **2** illustrate high pressure discharge lamps fabricated in accordance with the present invention. As shown in FIGS. **1** and **2**, a lamp **10** is fabricated from a first planar substrate **12** and a second planar substrate **14** which are bonded together by suitable means, as described below, and each lamp **10** comprises a plurality of cavities **18** which form individual luminescent micro-lamps. In FIGS. **1** and **2**, the cavities **18** are depicted as generally spherical and the substrates **12** and **14** are depicted as circular in plan view. It should be kept in mind that the cavities and substrates may be of any size and shape. The substrates are depicted as circular since handling equipment for circular plates is readily available from makers of integrated circuit manufacturing equipment. Cavities **18** may be square, rectangular, serpentine, elongated channels, or other shapes.

FIG. **1** illustrates a lamp constructed in accordance with the present invention in its simplest embodiment, that of an electrodeless RF activated lamp. The steps of manufacturing the lamp will also be discerned from this figure. Planar substrate **14** is transparent and consists of material suitable for containing the pressure and temperature of an operating lamp, one such suitable material is fused quartz. Cavity **18** which comprises a half cavity **20** in substrate **14** and a half cavity **22** in substrate **12** is formed by integrated circuit manufacturing techniques.

The upper surface **24** of un-etched substrate **14** is covered by suitable masking material, such as polysilicon, at the portions where etching is not desired, as etching will occur at the unmasked portions. Thereafter, the masked substrate is exposed to an etchant such as hydrofluoric acid for a time suitable to create cavity **20**. The time and amount of exposure to the etchant may be adjusted, in the known manner, to provide the cavity size and shape desired. Upper substrate **12** is also masked and etched in a similar manner to provide half cavity **22**. For most applications, substrate materials are commonly available with sufficient flatness (so called 10 micron flatness) such that they will bond by Van de Waal attraction. However, for certain bonding processes, it is desirable that the surfaces of substrates **12**, **14** that are to be bonded together be planarized. This can be accomplished by depositing phosphorus doped silicon dioxide and polishing the surface. Alternatively a smooth surface can be obtained by depositing phosphorous doped silicon dioxide and reflowing (heating) it.

After the formation of cavities **20** and **22** in substrates **12** and **14**, respectively, cavity **20** is charged with a suitable luminescent material. In this embodiment, the lamp is a mercury lamp so that an appropriate sized drop of mercury **28** (or mercury amalgam) is placed in cavity **20**. If cavity **18** is to be charged with a gas such as Argon, the bonding of

substrates 12, 14 may take place in an argon atmosphere at a pressure suitable for the final lamp. Accordingly, substrates 12 and 14 are placed in a pressure vessel at the appropriate argon pressure for the lamp to be manufactured. Thereafter, lower surface 26 of substrate 12 is bonded to upper surface 24 of substrate 14. The bonding interface 16 may be formed by any suitable means such as fusion or anodic bonding (as described above). After the bonding is completed, the completed lamp 10 is removed from the pressure vessel and cavity 18 will contain an argon atmosphere having a charge of mercury that will vaporize and form a mercury vapor lamp upon energization. Since this is an "electrodeless lamp", the mercury is vaporized and luminesces by application of RF energy from external RF electrodes 30 which may or may not be physically attached to the lamp. By the use of the wafer bonding process, each cavity 18 is individually sealed, that is, the substrates are chemically bonded to each other at all points of contact between the substrates.

FIG. 3 illustrates how the present invention is used to produce a lamp having electrodes which is a more common design than the RF lamp of FIG. 1. In FIG. 3, the same reference numerals are used to indicate the same structure that of FIG. 1. In FIG. 3, each half cavity 20, 22 in substrates 14, 12 is produced by masking and etching in a similar manner as the lamp of FIG. 1. After the etching of the half cavities 20, 22 a further manufacturing step takes place: the deposition of electrodes 40 and 42 in cavities 20, 22 respectively. The electrodes may be composed of any suitable electrode material, such as tungsten, and are deposited by known metal deposition processes, i.e. masking, etching and deposition of material. Since electrodes 40, 42 must be connected to current, electrical connection must be made to electrodes 40, 42. Connection with electrode 42 is made by etching a channel 46 in the upper surface 44 of substrate 12. In this case, upper surface 44 is masked at the areas to remain unetched and an etchant acts on the unmasked portions to etch channel 46 into surface 44 down to the electrode 42 to expose its rear surface. Thereafter, by deposition and patterning, a coating of conductive material 47, which may be a metallic or non-metallic conductor is applied in channel 46. Coating 47 extends from the electrode 40, 42 to the outer surface of the respective substrates. In order to maintain the pressure integrity of cavity 18, "plug" material 48 such as glass is deposited over metal layer 46 to strengthen cavity 18 and to render the outer substrate surfaces flush. Thereafter, substrates 12, 14 are charged with the appropriate fill or dosing material and bonded as is described above with respect to the lamp of FIG. 2. Connection of electrodes 40, 42 to an appropriate source of electric potential will cause the lamp to illuminate. Additional pairs of electrodes, such as starter electrodes, may also be deposited and connected in a like manner.

FIG. 4 illustrates another embodiment of the present invention in which the electrodes are disposed in side-by-side relationship, the same reference numerals are again used to denote similar structure. As shown in FIG. 4, the upper substrate 12 is formed in a similar manner to the previous embodiments. However, lower substrate 14 is first masked and etched so as to form a relatively wide rectangular cavity 60 and electrodes 62, 64 are deposited on its flat lower surface. A second deeper central cavity 66 is then etched into substrate 14 by suitable masking and etching techniques, and by use of an etchant which does not attack the material of electrodes, 62, 64. These electrodes will overhang cavity 66. Thereafter, the lower surface of substrate 14 is etched to create channels 68, 70 which contact the lower surface of electrodes 64, 62 respectively. A conductive layer 72, 74 may then be deposited in channel 68, 74 for electrical connection to electrode 64, 62. Thereafter, plug material 76, 78 may be used to fill in the gap between the lower surface of substrate 14 and metallic layers 72, 74. The cavity 18 is then charged. The lower surface of substrate 12 is then bonded to substrate 14 in the manner described above.

The present structure and methodology also lends itself to the manufacture of miniature fluorescent bulbs which utilize a phosphor coating which, when energized by the ultraviolet rays generated by mercury vapor, will fluoresce. In FIG. 4, a phosphor layer 80 is deposited on the upper surface of substrate 12. Such placement will prevent contamination from the mercury, as the external phosphor may easily be protected by a coating layer or an additional substrate. Alternatively phosphors could also be deposited within cavity 66. The lamp shown in FIG. 4 has both electrodes disposed in a single substrate and the electrical connections are made on a single substrate. It is also noted that in the construction of this type of lamp, there need not be a half cavity disposed in substrate 12 because if the portion of the cavity disposed in substrate 14 is large enough, upper substrate 12 may be merely a flat piece of fused quartz or other substrate material.

FIG. 5 shows yet another variant of the side electrode lamp of FIG. 4. In the lamp shown in FIG. 5, the lower substrate 14 further includes deposition of layers 82, 84 of P-glass (phosphorus doped glass) which cover electrodes 62 64- to a level equal to the upper surface of substrate 14. Thereafter, the upper substrate 12 has channels 86, 88 etched through substrate 12 and through the P-glass layers 82, 84 so as to expose the upper surface of electrodes 62, 64. Thereafter, conductive layers 90, 92 and plug material 94, 96 are deposited in channels 86 and 88. This arrangement permits contact with and connection to electrodes 62, 64 through the upper surface of the device rather than the lower surface of the device as shown in FIG. 4. The use of P-glass also provides an efficient sealing of the electrodes to the substrate.

FIG. 6 illustrates a side electrode lamp 100 which is constructed similar to that of FIG. 4 with the addition of melt zones 102, 104 which are used to further seal the electrodes within the substrates. Melt zones 102, 104 are formed by exposing the completed lamp to a CO_2 laser which will melt the fused quartz substrates to seal the tungsten electrodes firmly therewithin. Additionally, a layer of molybdenum may be added to the tungsten electrodes to aid in sealing. The molybdenum layer may be placed adjacent to the tungsten, in contact with the tungsten, or it may be deposited on top of the tungsten. The molybdenum layer will assist the substrate/electrode seal with or without melt zones 102, 104.

As noted above, lamps fabricated by this methodology may be any type of gas discharge lamp. The material suitable for the substrates is also not required to be fused quartz, as any transparent or translucent material capable of withstanding the heat and pressure generated by the particular lamp design (such as PCA or sapphire) may be used. In certain circumstances, glass (or quartz glass) is a suitable substrate for use with the certain types of lamps. The number of cavities disposed in the substrate may be varied in accordance with the requirements of the application. The lamps may be used as illumination or as display. Finally, the lamps can be energized all at once or circuitry can be disposed on the substrate so as to provide non-simultaneous activation of the various microlamps disposed in the substrate.

FIG. 7 illustrates a micro-laser constructed in accordance with the invention. Micro-laser 120 is constructed, as are the

previously-described gas discharge lamps, from an upper substrate **122** and a lower substrate **124**. Lower substrate **124** has a first, relatively shallow channel **126** disposed thereon and a second deeper channel **128** at its centermost portion, formed by etching and deposition techniques similar or identical to those described above. Extending into channel **128** are first and second electrodes **130**, **132**. Similarly upper substrate **122** has a channel **134** formed therein. Mounted to the exterior of substrate **124** is a partially reflective mirror **136** formed by metal deposition, photolithography, etching and other techniques. Disposed on the upper substrate **122** is a fully reflective mirror **138**. A central cavity **140** is formed by the half cavities **128**, **134** and may be charged with gaseous material which will last under application of electrical input applied to electrodes **132**, **130**.

When a discharge is created between electrodes **130**, **132** within cavity **140**, the action of mirrors **136** and **138** will provide a lasing action such as to cause the atoms of the gaseous material to lase as is known to those skilled in the art of gas discharge lasers. Thus, partially reflective mirror **136** and fully reflective mirror **138** form an optical cavity for the excitation of atoms of the gaseous fill material. Suitable gaseous fill material are those usually utilized in large size gas discharge lasers. Such material includes CO_2, Helium-Neon, Argon and the like. By suitable selection of the gaseous material and by the size and properties of the optical cavity, the lasing frequency may be adjusted over a wide frequency range. Such frequencies can range from the infrared to the ultraviolet. Gas discharge lasers are capable of generating light of a blue frequency or higher which, at this date, are difficult for solid state devices. Micro-lasers constructed in accordance with this invention can also be "electrodeless". Such lasers can be pumped through the application of external RF or microwave energy.

FIG. **8** shows another embodiment of a micro-laser constructed in accordance with the present invention. In FIG. **8** the same reference numerals are used to indicate the same structure as that of FIG. **7**. In the laser structure of FIG. **7**, mirrors **136** and **138** were disposed external to the substrates. The present invention does not require that the mirrors be disposed externally of the optical cavity. FIG. **8** illustrates a laser structure including mirrors disposed in cavity **140**. In FIG. **8**, a partially reflective mirror **144** is disposed on the lower surface of cavity **128** in lower substrate **124**. A fully reflective mirror **146** is disposed on the upper surface of cavity **134** in upper substrate **122**. The mirrors used in the structures of FIG. **7** and FIG. **8** may also be constructed from metallic materials which may be deposited within the substrates. It is to be further noted that the mirrors utilized in the micro-lasers of FIG. **7** and FIG. **8** need not have planar surfaces. The mirror surfaces could be curved in accordance with any special requirements. Furthermore, the mirrors can be spaced apart from the substrates and need not be mounted thereto. A particularly suitable substrate material for use in a laser device is sapphire. Since sapphire is crystalline, anisotropic etching can provide mirrors with superior optical qualities.

The present development is also adaptable for use with conventional, rather than deposited, electrodes. As shown in FIG. *9a*, a discharge lamp is constructed using conventional small electrodes. Lamp **160** includes an upper substrate **162** and a lower substrate **164** which may be of materials, as described above, which are suitable for withstanding the discharge conditions, such as glass, quartz or sapphire. Lower substrate **164** is masked and etched, in a manner similar to that described above, so as to provide a lower half cavity **166**. Thereafter, lower substrate **164** is masked again and etched so as to provide shallow trenches **170** on each side. Shallow trenches **170** are used to mount conventional electrodes **172** which consist of a molybdenum pad **174** welded or otherwise joined to a tungsten wire **176**. Tungsten wire portions **176** of electrodes **172** may have emitters such as thorium, barium titanate, barium zirconate or other emitter sources contained within (i.e. it is a composite material) or they may have emitter containing material welded onto the tips or coated on top. If the type of lamp requires it, a second pair of electrodes, such as starting electrodes, may be placed in trenches **168**, **170** before the bonding of substrates **162**, **164**.

Upper substrate **162** is masked and etched so as to provide an upper half cavity **178**. The mercury fill **180** is placed in half cavity **166** and thereafter upper substrate **162** and lower substrate **164** are bonded together, by a fusion bonding process in an argon (or other fill gas) environment. In this process the wafers are annealed in an appropriate high pressure atmosphere so as to counter the mercury pressure which increases due to the vaporization of the mercury upon annealing. The annealing process forms a permanent bond at the interface between substrates **162**, **164**.

After annealing, substrates **162**, **164** are then heated with a laser or a microtorch at melt zones **180** to seal the molybdenum pads **174** to substrates **162**, **164**. Thereafter, channels **182** are etched in the lower surface of substrate **164** and extend to electrodes **172** to permit lead wires **184** to be attached to the now exposed molybdenum portion **174** of electrodes **172**.

FIG. *9b* illustrates another "conventional electrode" lamp constructed in accordance with the present invention. FIG. *9b* illustrates a filamented, incandescent lamp **186**. The same reference numerals as used in FIG. *9a* are used to illustrate the same structure in FIG. *9b*. In FIG. *9b* molybdenum pads **188** are connected by a tungsten filament **190** when cavity **178** is charged with an inert gas, such as argon and a halogen to support the tungsten-halogen transport cycle, a halogen lamp is formed. Of course, many other types of filamented incandescent lamps may be utilized with the construction shown in FIG. *9b*.

Display Devices

FIGS. **10***a*–**10***d* illustrate a first construction for a flat panel gas discharge display in accordance with the invention. The display construction begins with a first translucent or transparent substrate **200** upon which a series of metal first electrodes **202** are deposited and which extend across what will be the surface area of the display. First electrodes **202** are deposited and patterned in the manner described above with respect to the manufacture of lamps. The choice of the metal to be used in first electrodes **202** is determined by the operating conditions of the discharge, and first electrodes **202** can be deposited by thick or thin film techniques. Thereafter, the surface of substrate **200** and first electrodes **202** is planarized by using planarizing techniques such as spin-on glass or the deposition of a phosphorous doped SiO_2 (p-glass) **204**, followed by an annealing step to harden same. The substrate, metal first electrodes **202** and planarizing layer **204** are shown in FIG. **10***b*.

Substrate **200** is then bonded to an intermediate substrate **206** in which a series of cavities (holes) **208** have been etched (or otherwise produced) with the same spacing as that of electrodes **202** (see FIG. **10***c*). The sidewalls of the etched cavities **208** may be deposited with a phosphor **210**, or other luminescent material, if required by the display. The bonding of substrate **200** to perforated substrate **206** is accomplished by wafer bonding techniques such as fusion bonding or anodic bonding (described in detail above). The wafer

bonding of substrates **200**, **206** will join them together at all points of contract, other than at holes **208**. After bonding of substrate **200** to substrate **206**, the planarizing layer **204** is removed in the area of cavities **208** over first electrodes **202** which will expose electrodes **202** in cavities **208** of the display. The planarizing layer **204** can be removed in cavities **208** by the usual masking and etching techniques using photolithography or it could be left unremoved with a discharge formed by capacitive coupling.

Thereafter a third substrate **212** is prepared. Patterned and deposited on substrate **212** are a second pattern of metal electrodes **214** which in the final form will extend perpendicularly (orthogonally) to first electrodes **202**. Substrate **212** is thereafter planarized with a planarizing layer **216**. A masking and etching step is then used to remove the planarizing layer **216** in the areas that will be within discharge cavities **208**. Finally, substrate **212** is wafer bonded to substrate **206** (which is already bonded to substrate **200**), to form the finished display. This final bonding is carried about in the ambient atmosphere which is to be sealed into the individual cavities (i.e., argon, xenon, neon and/or helium for a plasma display). Any other necessary dosing material can also be placed in cavities **208** prior to forming the final wafer bond. As is shown in FIG. **10***d* (which is a plan view of the finished assembly), the assembly consists of a plurality of cavities **208** disposed within the display with the electrodes **202**, **214** running perpendicular to each other and intersecting at cavities **208** (pixels). The width of electrodes **202**, **214** is exaggerated so as to illustrate the construction. In practice, electrodes **202**, **204** need not be as wide so as to not obscure the light emitted by individual cavities **208** (pixels). The three substrates may be formed by any suitable material such as glass, with quartz or sapphire utilized if the type of discharge requires it.

FIG. **11***a*–**11***d* illustrate a second construction for a gas discharge display in accordance with the present invention. This construction differs from that of FIGS. **10** in that the need for depositing planarizing layers is eliminated. As shown in FIGS. **11**, a first substrate **220** is etched with a series of trenches **222** in which are deposited first electrodes **224** as shown in FIG. **11***b*. Thereafter, substrate **220** is wafer bonded to a perforated second substrate **226**. Second substrate **226** contains a multiplicity of cavities **228** which will form the individual picture elements (pixels) of the display. The spacing between cavities **228** is the same as between electrodes **224**.

Third substrate **230** is prepared in the same manner as substrate **220**, that is a series of trenches **232** are etched therein and second electrodes **236** are deposited therein. Substrate **230** is wafer bonded to the upper portion of substrate **226** and is arranged so that first electrodes **224** are disposed orthogonally with respect to second electrodes **236**. Since the electrodes **224** and **236** are disposed in trenches, a proper sealing of cavities **228** is not accomplished by the wafer bonding of the three substrates together. The sealing of cavities **228** is accomplished by means of a CO_2 laser. As is seen in FIG. **11***d* laser seals **238**, **240** seal electrodes **224** to substrate **220** while laser seals **242**, **244** are utilized to seal electrodes **236**. The laser will melt and fuse the material of the substrates around the electrodes to seal each of the cavities. The laser is applied in the ambient atmosphere that is to be sealed within the cavities. The laser beam can be sharply focussed so that the melting of the substrate material takes place only at the aim points of the laser beam and does not affect the integrity of the display as a whole.

FIG. **12***a*–**12***e* illustrates yet another construction for a gas plasma display which utilizes two, rather than three, substrates and which disposes the electrodes along the side of the discharge cavities to minimize obstruction. In this construction, a first substrate **300** is patterned and etched with a series of trenches **302** in which a series of metal first electrodes **304** are deposited. As seen in the plan view of FIG. **12***e*, electrodes **304** have extensions **310** extending laterally therefrom. A planarizing layer **306** is then deposited over substrate **300** and electrodes **304**. Thereafter polysilicon masks **308** are deposited over the planarizing layer **306**. As shown in FIG. **12***b*, polysilicon masks **308** extend only partially over extensions **310** of electrodes **304**. As shown in FIG. **12***c*, half cavities **312** are then etched with the polysilicon masks **308** preventing etching thereunder. The etchant used is one which will etch the material of substrate **300** and planarizing layer **306** but does not substantially affect electrode **304**. As shown in FIG. **12***c* after the etching process and the removal of the polysilicon, electrode extensions **310** extend into individual half cavities **312**.

As illustrated in FIG. **12***c*, the finished substrate **300** has an upper surface which is planar, which permits direct bonding to a second substrate. As shown in FIG. **12***d*, a second substrate **320** is prepared in a similar manner to that of substrate **300** in that it is etched with a series of trenches **322** and deposited with second electrodes **324** which have a L-shaped extension **326** (see FIG. **12***e*). Thereafter, a planarizing layer **328** is deposited over electrodes **324** and a polysilicon mask (not shown) is applied which is used to mask the etching of second half cavities **330** in the same manner as described above with respect to substrate **300**. After preparation of substrate **320**, substrate **300** is wafer bonded to substrate **320** to form the finished sealed cavities as shown in FIG. **12***d*. As is seen in the top view of FIG. **12***e*, a plurality of cavities are formed which have electrodes extending laterally thereinto. It is seen that in this view, the electrodes obscure very little of the individual cavities which permits greater brightness from the resulting matrix of pixels forming the display. This construction makes use of planarizing layers, however it is to be noted that the planarizing layers could be omitted and the cavities sealed by laser application as described above with respect to the display of FIGS. **11**.

As is seen, the completed panels have upper and lower electrodes arranged orthogonally with respect to each other, i.e. in a row and column arrangement. This arrangement permits each discharge cavity (pixel) to be individually activated (addressed) thus these displays can be used for information or video display purposes. Since each cavity can be individually doped prior to final sealing, appropriate dopants to create various colors or three colors (red, green and blue) for full color displays may be utilized with this technology. Since the cavities will easily contain high pressures greater brightness can be achieved.

Vacuum State Devices

As shown in FIGS. **13***a*–*f*, the construction of a vacuum microelectronic device begins with a first substrate **402** which will form one half of the device. Substrate **402** may be of any material suitable for use in a wafer bonding process. It is noted that substrate **402** need not be transparent, as is the case with respect to light emitting devices, as transparency is irrelevant to operation of an electron tube. Accordingly, substrate **402** can, for example, be quartz, sapphire, silicon or glass depending upon the anticipated operating conditions of the device. As is seen in FIG. **13***a*, a cathode **404** (electron emitter) is deposited and patterned on substrate **402**. As seen in the top view of FIG. **13***a*, cathode **404** comprises end pads **406** and a serpentine active portion **408** joining the end pads. Cathode **404** is formed

from a suitable electron emitting material, for example, a metal such as tungsten, molybdenum, other refractory metal or silicide. The serpentine configuration of portion 408 of cathode 404 serves both to increase the area for electron emission as well as to form an electrical resistance element to provide heating to promote electron emission. If necessary, a further coating on top of cathode 404 may be made to increase its electron emission or to facilitate its heating.

Coating

As is seen in FIG. 13b, deposited over substrate 402 and cathode 404 is an intermediate layer 410 of silicon dioxide (SiO_2) which may be deposited by any suitable deposition method such as CVD, PECVD, SILOX or others. Thereafter deposited on silicon dioxide layer 410 is a metal layer which is patterned to form a grid 412. As is seen in the top view of FIG. 13b, grid 412 includes a generally rectangular portion 414 with elongated slots 416 and 418 and a contact pad 420 joined to portion 414 by a bridging member 422. This particular shape of grid 418 may be made by conventional patterning processes, for example, photolithographic masking and etching. Furthermore, the grid may take any appropriate shape for the projected use of the device. It is only necessary that the grid be configured to permit the flow of electrons therethrough, as it functions as the electron modulating structure in a vacuum device. The thickness of silicon dioxide layer 410 defines the cathode-to-grid spacing, and may be adjusted in accordance with the proposed use and electrical requirements of the device.

After deposition of grid 412, the substrate and deposited electrodes are planarized with a layer 424 of glass suitable for the bonding process, for example, by the deposition and reflowing of a second intermediate layer 424 of borosilicate glass or phosphorosilicate glass, or by any other planarizing method. Thereafter, a cavity 426 is etched through the planarizing layer 424, silicon dioxide layer 410 and substrate 402, using a selective etchant that leaves grid 412 and cathode 404 unaffected. As is seen in FIG. 13c, the cavity 426 and its associated electrodes is sized so that outermost portions of cathode 404 and grid 412 extend into the lateral surface of the cavity. Cavity 426 and its associated electrodes may be adjusted in size from micron size to many millimeters depending on the application of the device.

A second substrate 430 forms the other half of the vacuum microelectronic device. Substrate 430, which may be the same or dissimilar material from that of substrate 402 (so long as it is suitable for wafer bonding to the first substrate) has a trench 432 etched therein. Patterned and deposited in trench 432 is anode 434 which in operation serves to collect the electrons emitted by cathode 406, as modulated by grid 412. As seen in the top view of FIG. 13d, anode 434 comprises a rectangular portion 436 and a contact pad 438 interconnected by a bridge 440. After deposition of anode 434 in trench 432, trench 432 is filled in with a deposit of planarizing material 443, and the upper surface of substrate 430 is restored to planarity. Thereafter, a cavity 444 is etched into the surface of substrate 430 and beneath anode 434. Cavity 444 is narrower than trench 432 so that anode 434 will be embedded in the side walls of cavity 444. After the etching of cavity 444, the second substrate 430 will appear as shown in FIG. 13(e).

Thereafter, substrate 430 is inverted, aligned and wafer bonded to substrate 404 in a vacuum environment. The wafer bonding process may be either fusion or anodic bonding, as described previously, and results in a bond across the entire interface 445 between substrates 402, 430, which bond has a strength comparable to that of the bulk material. In order to make contact with the now embedded electrodes, contact holes are made in the substrates by either etching or "drilling" with a laser. As shown in FIG. 13f, the contact holes 448 extend to contact pads 406 of cathode 404. Contact hole 450 (see top view) extends to contact pad 420 of grid 412 and a contact hole 452 extends to contact pad 438 of anode 434. Thereafter, conductive material is placed in openings 448, 450, 452 to provide electrical contact with the associated electrodes.

FIG. 14 illustrates an integrated arrangement of four microelectronic vacuum devices 462, 464, 466 and 468 on a single substrate 460. In this illustration only four separate devices are shown. However any number of devices may be placed on a single substrate dependent upon the needs of the circuit in question. Furthermore, conductive lead traces 470 similar to that of a printed circuit board may be placed on the surface of substrate 460 to interconnect the devices. The conductive traces could also be disposed on one of the substrates before the substrates are bonded together. As shown in FIG. 14, devices 464, 466 have their various electronic elements interconnected. Device 468 remains alone and may be accessed separately by conductive leads 472 leading to the other circuit components of the total device. Thus, the present invention provides an integrated vacuum device suitable for use with a variety of electronic circuits. The size, configuration and number of vacuum state devices may be varied to suit the electronic needs of the circuit in question.

Through deposition of further metallic and planarizing layers vacuum devices having more than one grid (tetrodes, pentodes, etc) may be constructed.

FIG. 15 illustrates a vacuum microelectronic device 478 based upon field emission rather than thermionic emission. In this device, the same reference numerals are used to illustrate the same structure as in FIG. 13. In this device, cathode 404 is replaced with a cathode 480 which has a series of tips 482 for emitting electrons. The grid and the anode are basically the same.

The above described structures and methodology are merely illustrative of the principles of the present invention. Numerous modifications and adaptations thereof will be readily apparent to those skilled in the art without departing from the spirit and scope of the present invention and the appended claims. For example, the cathode, the anode, or both of these electrodes may be in contact with the bottom of the cavity, as shown in the variations shown in FIGS. 16a–e; wherein in each variation, the first substrate 500 is bonded to the second substrate 510 to form a sealed cavity 520, within which is located cathode 530, grid 540 and anode 550. Of course, access to any of the electrodes may be via the bottom of the first substrate, as well as via the top of the second substrate. Finally, it will be appreciated that in any of the various device constructions shown, the cathode and anode positions may be reversed.

What is claimed is:

1. A vacuum state electronic device comprising:

first and second substrates, each substrate having a contacting surface;

at least one cavity disposed in at least one of the substrates, said cavity having an opening in the contacting surface of the at least one substrate, and said cavity containing a vacuum;

an electron emitting electrode disposed within the cavity;

an electron receiving electrode disposed within the cavity;

at least one electron modulating electrode disposed between the electron emitting electrode and the electron receiving electrode for modulating the flow of electrons therebetween;

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the first and second substrates being joined together across their respective contacting surfaces to seal the cavity.

2. The electronic device as claimed in claim **1** wherein at least one of the electrodes extends beyond the walls of the cavity into at least one of the substrates.

3. The electronic device as claimed in claim **1** wherein the electron emitting electrode has a serpentine configuration in plain view.

4. The electronic device as claimed in claim **1** wherein the electron modulating electrode has a generally rectangular configuration in plain view with at least one slot disposed therein to permit electrons to pass therethrough.

5. The electronic device as claimed in claim **4** wherein the electron modulating electrode includes first and second slots.

6. The electronic device as claimed in claim **1** wherein the electron receiving electrode is generally rectangular in plan view.

7. The electronic device as claimed in claim **1** wherein at least one of the electrodes includes at least one contact pad disposed within at least one of the substrates for electrical connection thereto.

8. The electronic device as claimed in claim **7** wherein at least one of the substrates includes at least one aperture leading from the surface thereof to one or more contact pads.

9. The electronic device as claimed in claim **8** further including conductive material disposed in the aperture for providing electrical connection to the pad.

10. The electronic device as claimed in claim **1** further including a second cavity having a second set of electrodes disposed in the substrate.

11. The electronic device as claimed in claim **10** further including conductive leads disposed along the surface of at least one of the substrates.

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